Technical Reference Guide
For SanDisk's MultiMediaCard

MultiMediaCard Parameters

Q: What is the difference between the MultiMediaCard terms and functions Idle , Inactive, Standby and Sleep?

A: Idle, Inactive and Standby are basically "protocol states" and not "electrical" states. Each of these states are described in Figure 5-1 of section 5.2 of the MultiMediaCard Product Manual. All of these "states" (excep for Sleep) have no meaning in SPI mode.

Idle: Entered from Command 0 and remains until a valid Command 1 response. MultiMediaCard mode only

Inactive: Entered from incompatible voltage range response via Command 1 or directly from Command 15. Exited only through power cycle. MultiMediaCard only.

Standby: The state where the card is "Ready" for the next command but not processing. Entered after any start bit is detected on the bus. MultiMediaCard mode only.

Sleep: SanDisk's electrical, power saving mode. This mode is the lowest power mode for the MultiMediaCard. It is entered automatically if no command is received within 5 msec. Exiting Sleep mode will occur automatically upon receipt of any command. Entering and exiting sleep mode is an automatic functio of the card and transparent to the host.

Q: What is the expected "Block" programming time?

A: The time it takes to program a SanDisk memory is somewhat variable. To explain the variation one needs to understand the nature of a SanDisk memory cell. Erase and programming time for each cell may vary due t temperature, voltage and age of that cell. SanDisk's internal erase and programming controller routines are apdative to meet and compensate for the factors described above, to ensure valid data is stored.

What SanDisk specifies is the average read/write or write/read time. This time is obviously dependent on t MultiMediaCard's clock signal from the host , but, the "maximum" Write speed is ≈ 200K Bytes/sec. and 1MB/sec. at 20MHz.

The second set of values that SanDisk provides are described in the "Read, Write and Erase Time-out Conditions" section (5.4.4.2) of the SanDisk MultiMediaCard Product Manual. is total Read time for data transfer (N_{AC}). N_{AC} is the sum of TAAC (bits 119 - 112) and NSAC (bits 111 -104) of the MultiMediaCard's CS register.

If TAAC = 26 hex (0010 0110 bin), then the time exponent = 6 (1mS) and the time mantissa = 2 (1.2) for a total asynchronous access time of 1.2m Sec. If NSAC = 00 hex (in hundreds of clock cycles) then the total time (N_{AC} is still TAAC + NSAC or 1.2m Sec. This time can be interpreted as a typical delay for the first data bit of a block.

The total Block programming time = N_{AC} * R2W_FACTOR (CSD bits 28 – 26). Following the existing exampl if R2W_FACTOR = 4 hex (100 bin), which translates to a multiple of 16 fromTabel 5-24. This makes the Wr time = 19.2m Sec.

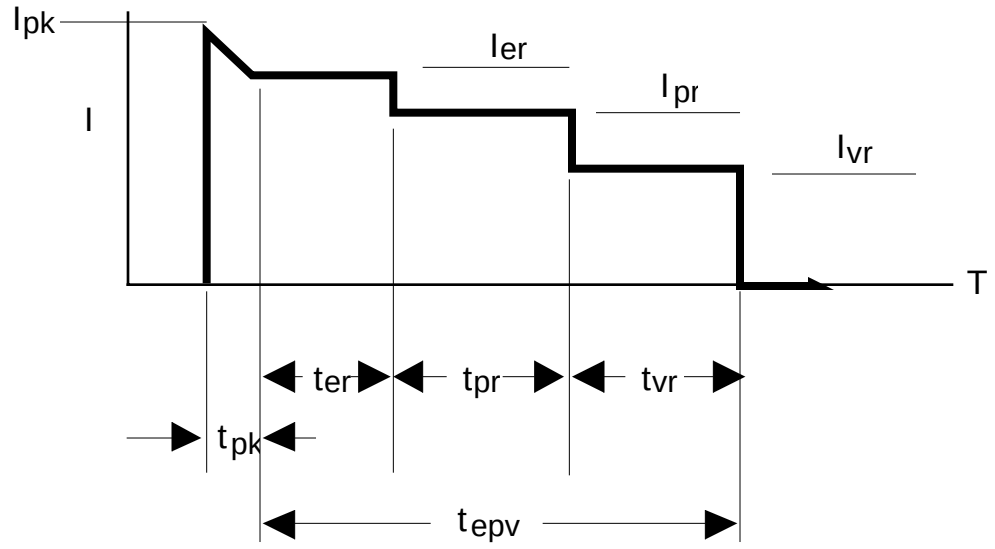
The values above are "typical" values. Worst case timeouts can be calculated from these values by multiplyi them by 10 in accordance with section 5.4.4.2 of the SanDisk MultiMediaCard manual.

Q: What is the absolute maximum (peak) current at either a power on cycle or a hot insertion.

A: The measured maximum peak current (as of 3/99) is 1.9A for 500nSec @ 2.7V and 2.1A for 500nSec @ 3.3V. This is a short current induced by the filter capacitors on the card. These currents exist for an extremely short time and are likely to improve as the product matures.

Other "Maximum Current" values can be found in the MultiMediaCard's CSD register.

Max. Value Name	CSD bits	Symbol	Value (as of 3/99)
Read Current	58 – 56	-	35ma
Write Current	52 – 50	-	45ma
Peak Current	-	Ipk	< 60ma
Erase Current	-	Ier	≈ 37ma
Program Current	-	Ipr	≈ 35ma
Verify Current	-	Ivr	≈ 25ma
Peak Current Time	-	tpk	> 1µSec
Erase Current Time	-	ter	≈ 0.5mSec
Program Current Time	-	tpr	≈ 1.5 to 3.5 mSec
Verify Current Time	-	tvr	≈ 1.5 to 3.5 mSec
Erase to Verify Time	-	tepv	≈ 3 to 7 mSec



These values describe Read and rite currents but, not the maximum "power on" current.
Empirically, cards have not exceeded 60mA at power up or during hot insertion and these "peaks" have not maintained these current levels for more than ≈ 1µSec.

Q: What is the (average or peak) current draw during the 74 (or 80) initialization clock cycles?

A: 2.5mAmps average (5mAmp peak) for the first 64 clocks and then it to sleep current.

Q: In the case of ATA products (CF and ATA), a power cycle (ramp up time, etc.) is defined in the PCMCIA specification. Is there a (similar) recommended power cycle timing profile for the MultiMediaCard?

A: t is not defined in the current MultiMediaCard standard, but, it may be in the future.

For the power supply SanDisk is using the voltage rise time is 1.5uSec.
Current consumption:

1.1A for 500nSec @ 3.3V
0.6A for 500nSec @ 2.7V

Q: What is the maximum ESD rating for the MultiMediaCard?

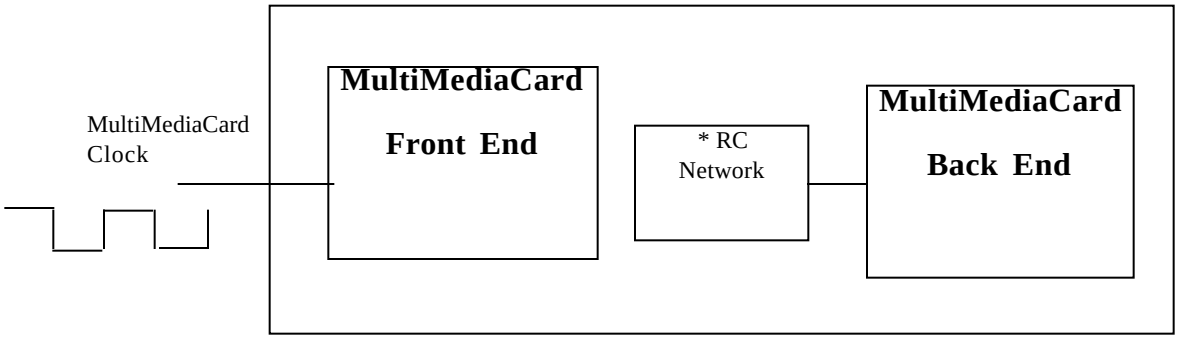
A: At this time the absolute maximum ESD value has not been measured, but, cards have been tested against the "Human Body" contact limit model. SanDisk cards meet and / or exceed the ± 4KV in accordance with MMCA spec. 1.4.

All tests were taken from the Electrostatic Discharge Association's Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBN) Component Level, document ESD STM5.1-1998.

Q: How is the Host MultiMediaCard clock synchronized / related to the Internal MultiMediaCard clock and can there be MultiMediaCard internal operations without the External clock?

A: There are two functional parts to MultiMediaCard controller. The MultiMediaCard "Front End" is controlled by the Host's clock signal to the card and the MultiMediaCard's "Back End" is controlled by an internal clock generated via an RC network. These two clocks are independent of each other. The RC network clock only requires power to be applied to the card and stops during sleep mode . Both clocks are Asynchonous.

"Front End" functions primarily deal with the "Host" interface and communications. "Back End" functions primarily deal with internal controller register functions, Flash Memory communications as well as Flash Memory itself. Internal "Back End" functions can and do continue while the MultiMediaCard Host clock is stopped.



**RC Network is ON or OFF depending on "Sleep" mode*

Q: Can the external "Host" clock frequency be increased / decreased in the normal course of operation?

A: Yes. The limits and restrictions are outlined in the SanDisk MultiMediaCard Product Manual, section 5.4. for Clock control. Briefly, the clock can be changed as long as the duty cycle is ≈ 50% and under 20Mhz or risir edge to rising edge is not less than 50nSec. Exchanges are on 8 clock cycle boundaries and a minimum of 8 clock cycles follow any operation.

Q: What are some the limiting factors are for higher speed transfers in open drain mode?

A: Open Drain mode is necessary for a multiple MultiMediaCard bus so that any card on the bus can respond without having to "drive" all cards. This usually means that the bus will need to run slower than the maximum speed since the rise time for the outputs are dependent on external pull-up resistors and multiple ca capacitances. Two factors may cause problems in higher speed systems.

1. Data transfer requencies that are too high might begin to "round" or attenuate the data's rising (c falling) edges causing data miscues.
2. The Host might not detect "slow" cards. The maximum Data Transfer Speed is a parameter of the MultiMediaCard's CSD register. SanDisk's cards can operate at the maximum allowable transfe rate according to the MultiMediaCard System Specification (rev. 1.4). Every card on the bus may not be a SanDisk card and may have a "slower" maximum data transfer speed. The MultiMediaCard System Specification (rev. 1.4) allows any MultiMediaCard to define it's own maximum data transfer speed in bits 103 to 96 of the CSD up to 20MHz.

   For SanDisk's MultiMediaCard, TRANS_SPEED from the CSD = 2A hex. The rate exponent (bits - 0) becomes 2 (or 10M bits / Sec.) and the time mantissa (bits 6 - 3) becomes 5 (or 2.0).

   10Mb/s * 2.0 = 20MHz.

As long as the host can send data at the maximum transfer rate, there are no issues for an MultiMediaCard operating in SPI mode. SPI mode operates in push-pull mode only.

Q: What is the SPI Maximum data transfer / clock speed for SPI mode?

A: The Maximum data transfer / clock speed is a "card" parameter not a protocol parameter. This means tha MultiMediaCard mode and SPI mode have the same maximum data transfer /clock speed of 20Mhz. The only difference is in the method used to access the data. MultiMediaCard mode may have protocols, like stream mode, that are able to provide more sequential data and speed up data access, but, the clock speeds and limits are identical in both modes.

Q: How are the bits / bytes read serially from the CSD register?

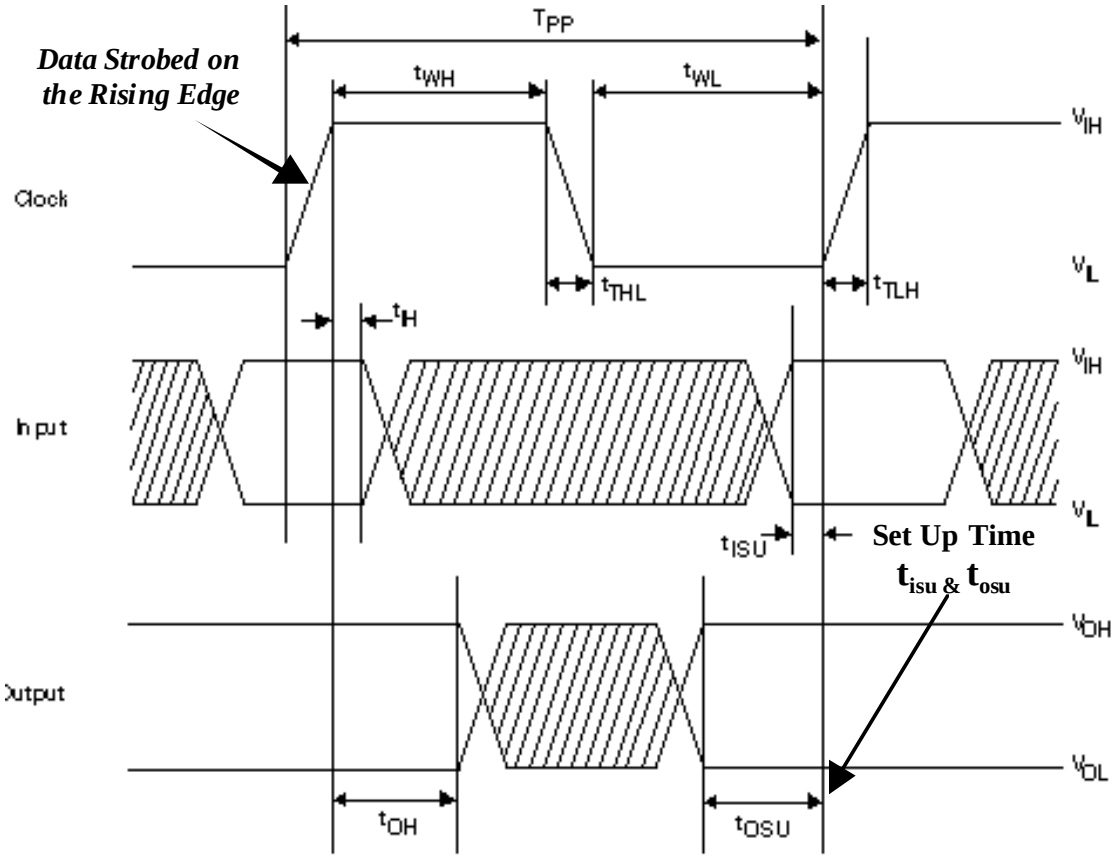
A: The data is read Most significant bit of the Most significant byte to Least significant bit of the Least significant byte. In other words, bit 127 of the CSD is shifted out first after a SEND_CSD command (CMD9) i issued. Currently, the first valid CSD bits (127 & 126), CSD_STRUCTURE, to appear for all SanDisk cards is bit 127 first as '0' followed by bit 126 as '1'.

Q: What is the expected (typical) gate size for both the MultiMediaCard port & SPI port in the verilog model?

A: 8K gates for logic and registers (command and response FIFOs included). Data buffers are excluded.

Q: Referring to the Bus Timing section 4.4.1.2.3 of the MultiMediaCard product manual, where is Data actually transferred?

A: Data is valid for both input and output on the MultiMediaCard clock's rising edge. Valid data is held for minimum of 3nS (t_{IH}) for input and 5nS (t_{IH}) for output.



Note: Data in the shaded areas is not valid.

Q: In Stream mode (CMD20) for the MultiMediaCard, how long do you wait after a Stop command (CMD12) t send the next command?

A: 8 clock cycles.

Q: Will there be a "lag" time after a Stop command (CMD12) is issued in Stream mode (CMD20)?

A: Yes, the time will be about 50 to 60 clock cycles from the time the Stop command is issued. Data transfer will stop upon detection of the Stop command.

Q: How much delay or how many clocks are required between SPI commands?

A: 8 Clocks. This value is referred to as NRC in section 6.4.3 (Table 6-2, Timing Constant definitions) in the MultiMediaCard Product Manual.

Q: How much delay or how many clocks are required between de-assertion of the SPI, CS line to the next assertion of the CS line in SPI mode?

A: Zero delay. You can raise the CS in one cycle and assert it again the next cycle.

However, There must be an 8 clocks delay between commands (end of response to start of command) and the sta bit of a command must be byte aligned to the CS.